

## TRANSMITTAL

Electronic Version v1.1

Stylesheet Version v1.1.0

### Title of Invention

METHOD FOR SEPARATELY OPTIMIZING THIN GATE DIELECTRIC  
OF PMOS AND NMOS TRANSISTORS WITHIN THE SAME  
SEMICONDUCTOR CHIP AND DEVICE MANUFACTURED THEREBY

Application Number :

Date :

First Named Applicant: Anthony I-Chih Chou

Confirmation Number:

Attorney Docket Number: FIS920030228US1

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Documents being submitted:	Files
us-fee-sheet	FIS920030228US1-usfees.xml us-fee-sheet.xml us-fee-sheet.dtd
us-ids	FIS920030228US1-usidst.xml us-ids.dtd us-ids.xml
us-request	FIS920030228US1-usrequ.xml us-request.dtd us-request.xml
us-assignment	FIS920030228US1-usassn.xml us-assignment.xml us-assignment.dtd FIS920030228US1Assignment1.tif FIS920030228US1Assignment2.tif FIS920030228US1Assignment3.tif
us-declaration application-body	FIS920030228US1Declaration1.tif FIS920030228US1-trans.xml us-application-body.xml application-body.dtd wipo.ent mathml2.dtd mathml2-qname-1.mod isoamsa.ent isoamsb.ent isoamsc.ent isoamsn.ent isoamso.ent isoamsr.ent isogr3.ent isomfrk.ent isomopf.ent isomscr.ent isotech.ent isobox.ent isocyr1.ent isocyr2.ent isodia.ent isolat1.ent isolat2.ent isonum.ent isopub.ent mmlextra.ent mmlalias.ent soextblx.dtd FIS920030228US1Drawing1.tif FIS920030228US1Drawing2.tif FIS920030228US1Drawing3.tif FIS920030228US1Drawing4.tif FIS920030228US1Drawing5.tif

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us-declaration	FIS920030228US1Declaration2.tif
us-declaration	FIS920030228US1Declaration3.tif
us-declaration	FIS920030228US1Declaration4.tif
<b>Comments</b>	
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